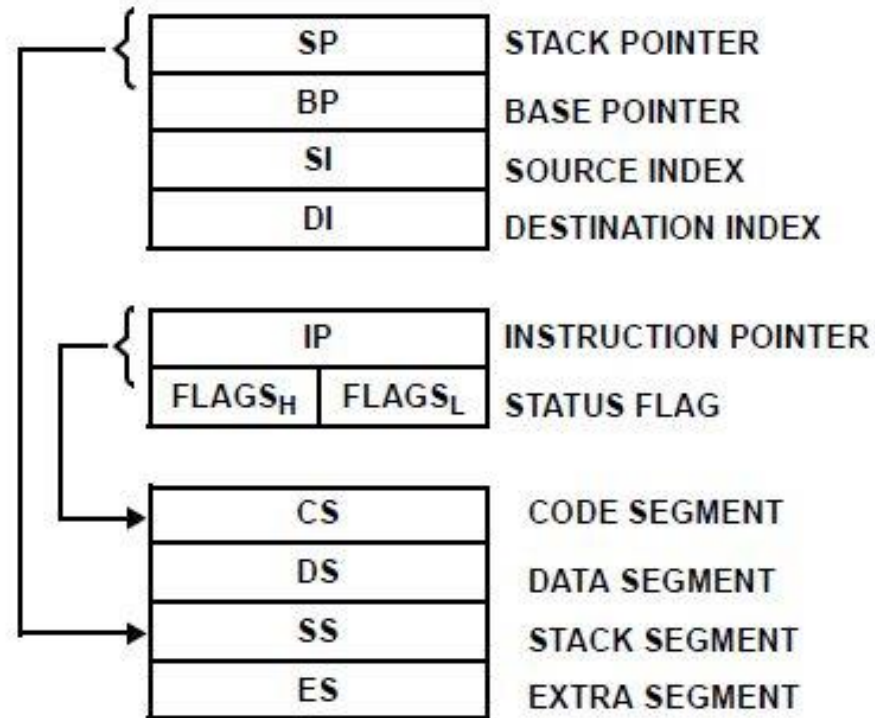


REAL MODE x86

AX	AH	AL	ACCUMULATOR
BX	BH	BL	BASE
CX	CH	CL	COUNT
DX	DH	DL	DATA

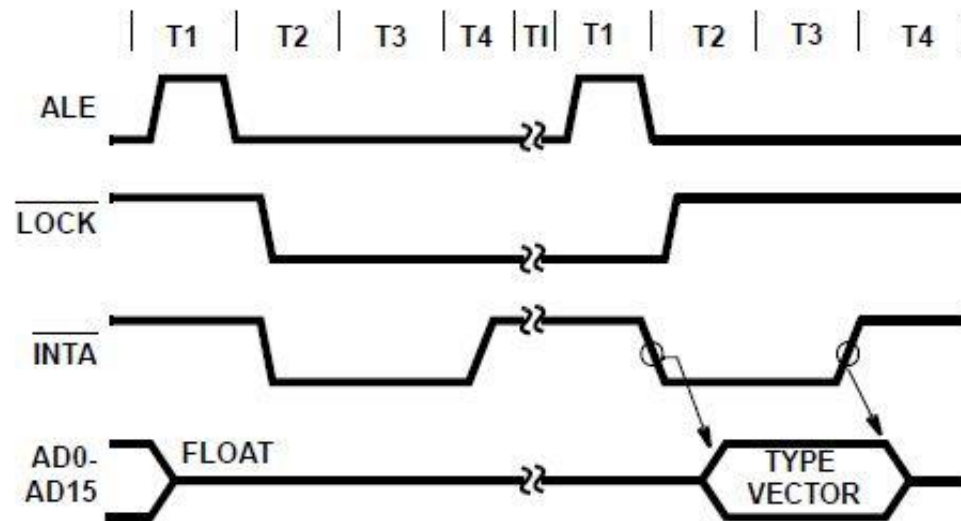


REAL MODE x86

- INICIALIZÁCIA PROCESORA
- 16-BITOVÝ REÁLNY MÓD
- FYZICKÁ ŠTARTOVACIA ADRESA
- V/V PRIESTOR

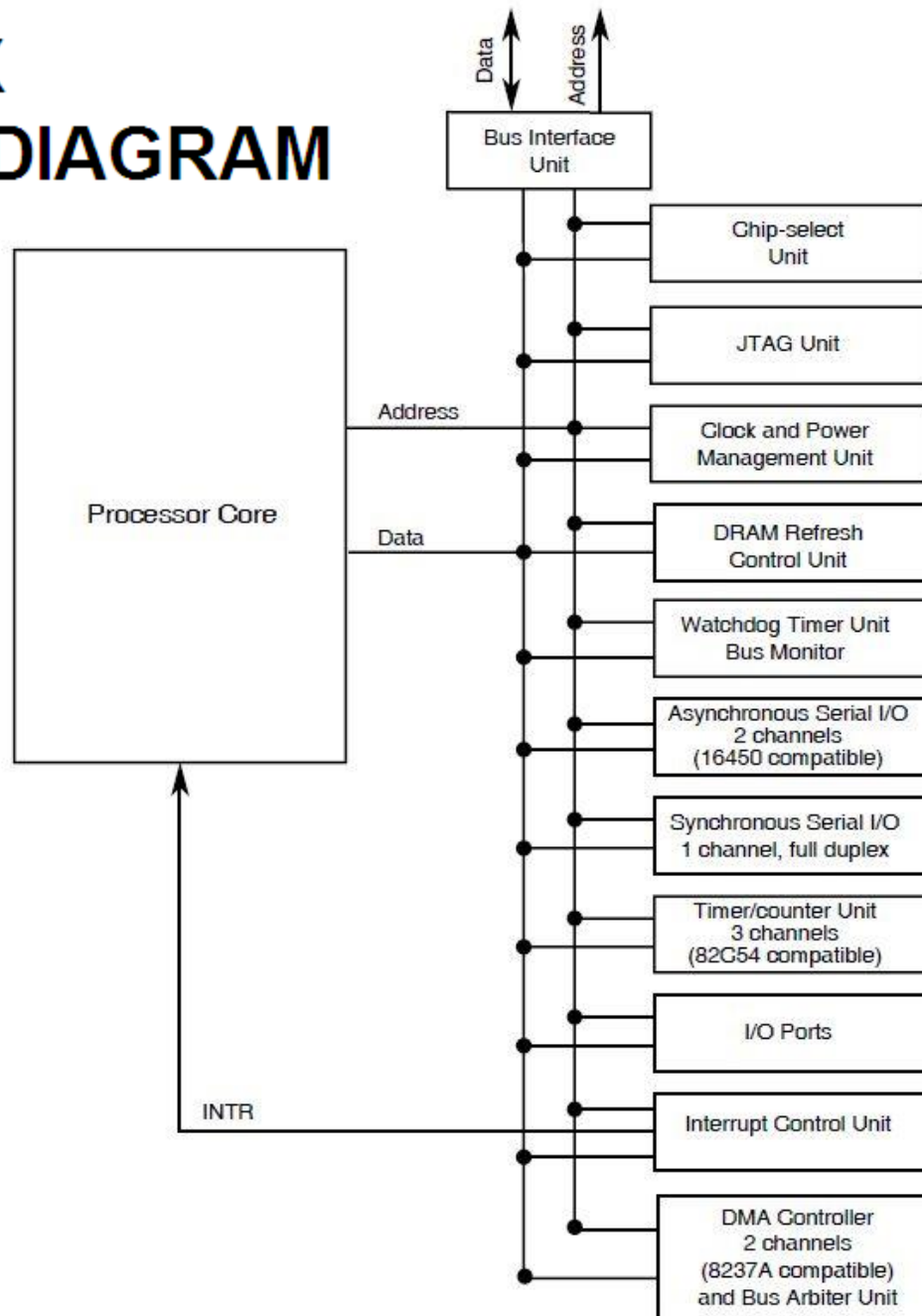
- HARDVÉROVÉ A SOFTVÉROVÉ PRERUŠENIE

REAL MODE x86



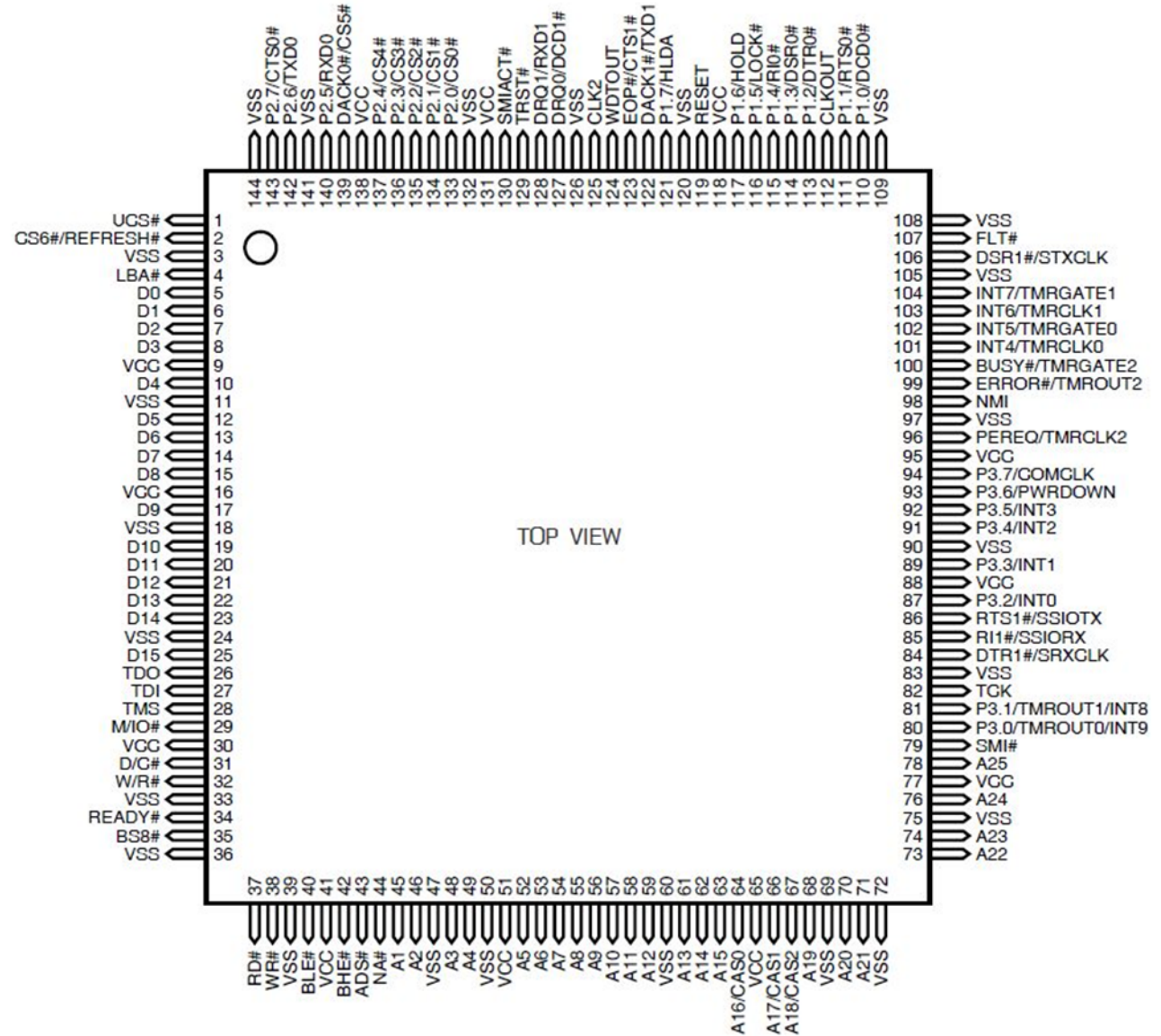
- **VEKTOR A ŠTARTOVACIA ADRESA
OBSLUŽNÉHO PODPROGRAMU**

80386EX BLOCK DIAGRAM



80386EX

PINOUT



80386EX

VYBRANÉ SIGNÁLY

CLK2	A25 -1
	BHE#
	BLE#
RESET	D15 - 0
	ADS#
READY	RD#
	WR#
	M/IO#
INT9 - 0	UCS#
BS8#	CS6# - 0#
	CAS2-0

80386EX

PROGRAMOVATELNÝ DEKÓDER (CHIP Select Unit)

- **UCS#, CS6# - CS0#**
- **15-bit CHANNEL ADDRESS**
- **15-bit MASK ADDRESS**
- **26-bit ACTIVE ADDRESS**

SYSTÉM NA BÁZE 80386EX

- **Frekvencia hodín procesora 25 MHz**
- **Signál RESET (tlačidlo a nábeh NN)**
- **Signál NMI (ošetrené tlačidlo)**
- **128 kB 8-bitovej pamäte EPROM**
(1x 27C1001, boot, interný dekóder)
- **64 kB 16-bitovej pamäte RWM**
(2x 62256, vektory, interný dekóder)

SYSTÉM NA BÁZE 80386EX

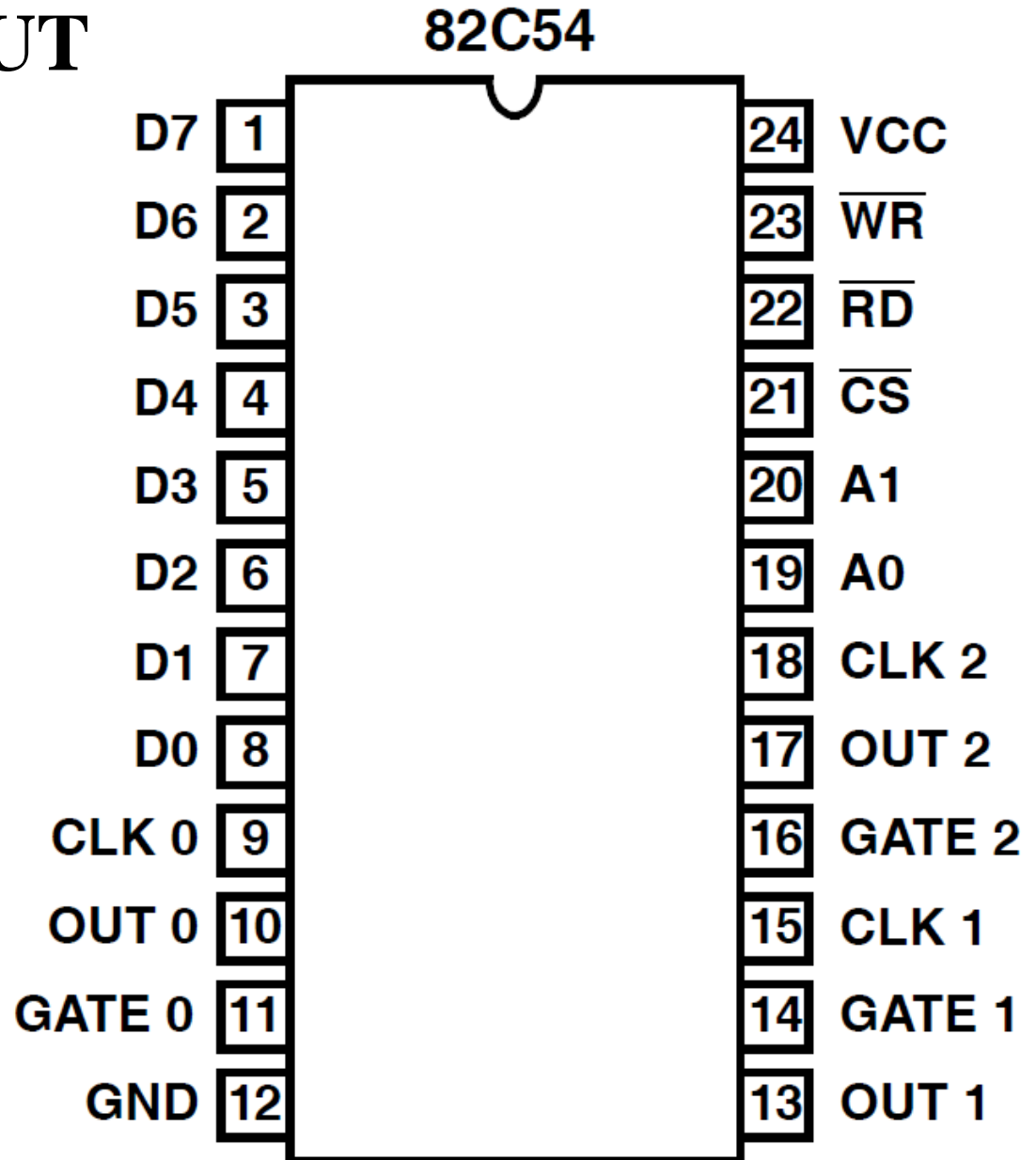
Externý úplný dekóder:

- **128 kB 8-bitovej pamäte EPROM
(1x 27C1001, boot)**
- **64 kB 16-bitovej pamäte RWM
(2x 62256, vektory)**

PERIFÉRNE OBVODY PRE x86

- **82C54**
- **82C55**
- **16C550**
- **82C59A**

8254 PINOUT



8254 CONTROL WORD (8253)

$A_1, A_0 = 11; \overline{CS} = 0; \overline{RD} = 1; \overline{WR} = 0$

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC - SELECT COUNTER

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW1	RW0	
0	0	Counter Latch Command (See Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

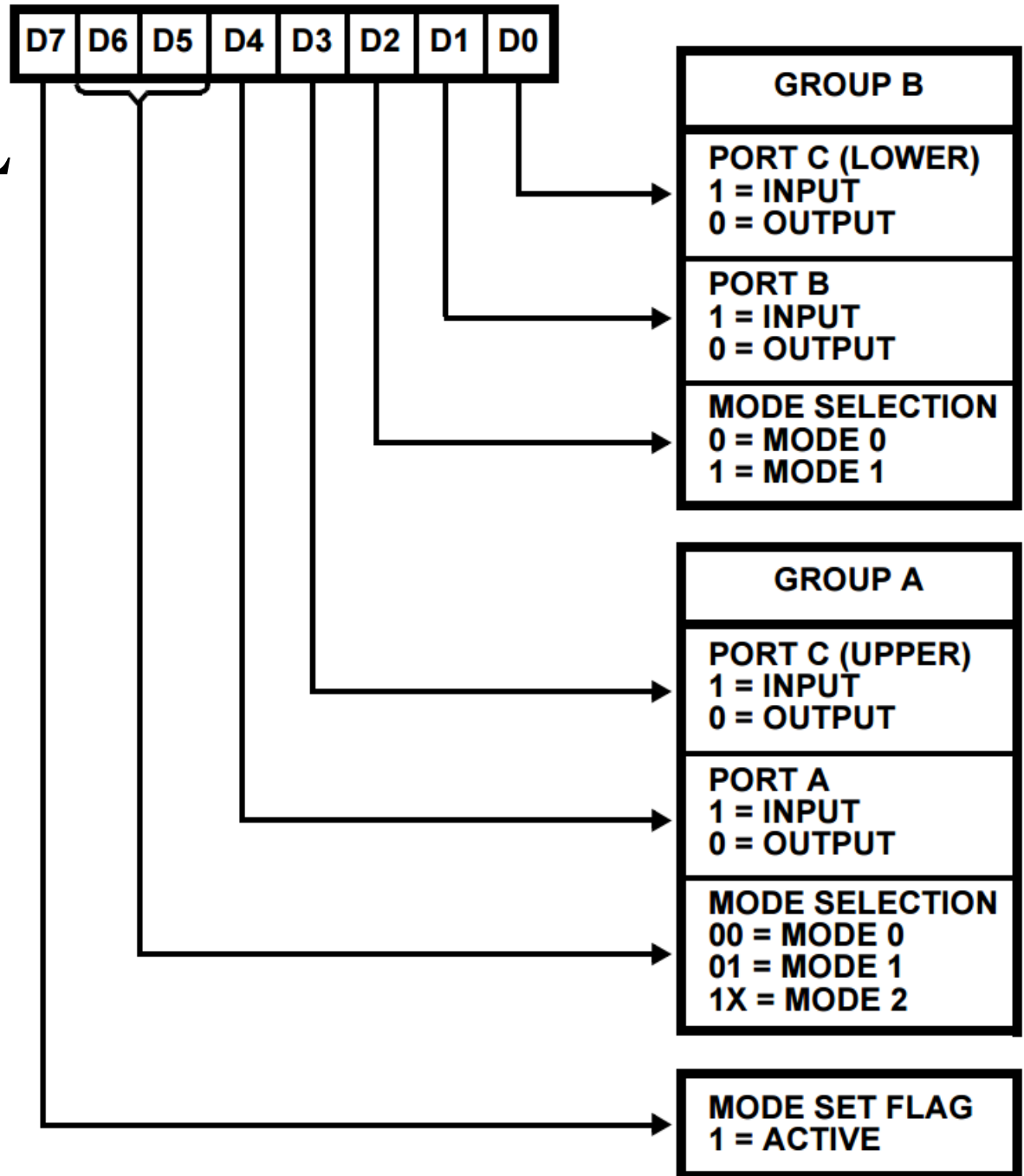
M - MODE

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

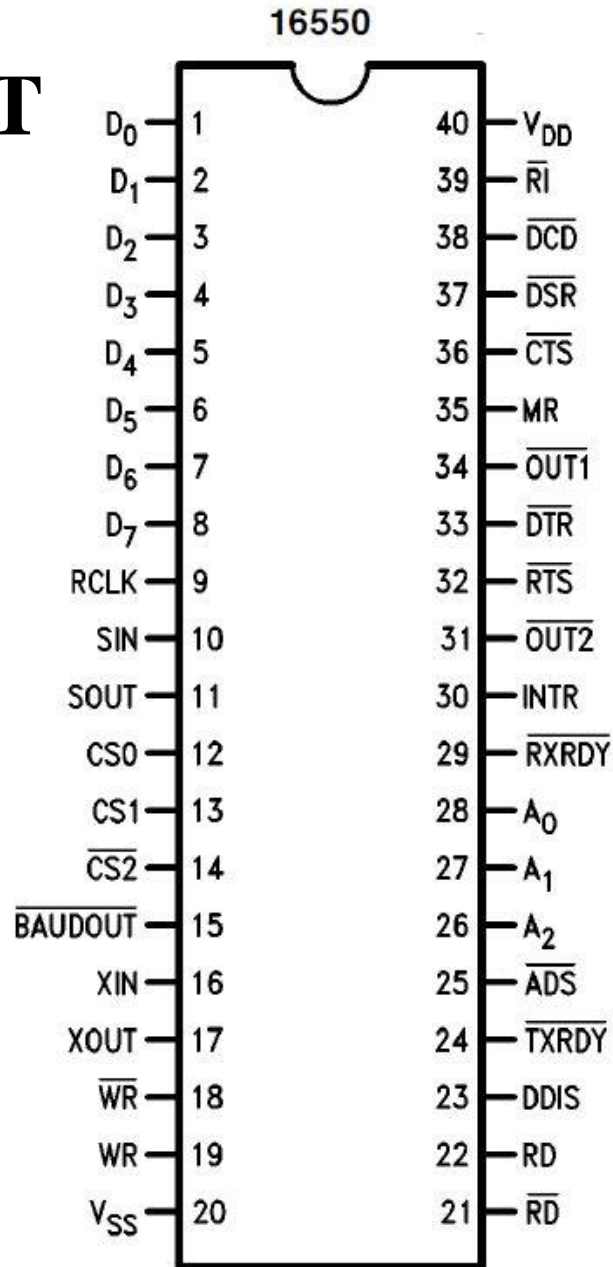
BCD - BINARY CODED DECIMAL

0	Binary Counter 16-bit
1	Binary Coded Decimal (BCD) Counter (4 Decades)

8255 CONTROL WORD



16550 PINOUT



Register Addresses

DLAB	A ₂	A ₁	A ₀	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Line Control Register

DL	SB	ST	P	PE	S	L1	L0
-----------	-----------	-----------	----------	-----------	----------	-----------	-----------

FIFO Control Register

RT1	RT0	0	0	DMA	TRS	RRS	FEN
------------	------------	----------	----------	------------	------------	------------	------------

Interrupt Control Register

0	0	0	0	EM	EL	ET	ER
----------	----------	----------	----------	-----------	-----------	-----------	-----------

Line Status Register

ER	TE	TH	BI	FE	PE	OE	DR
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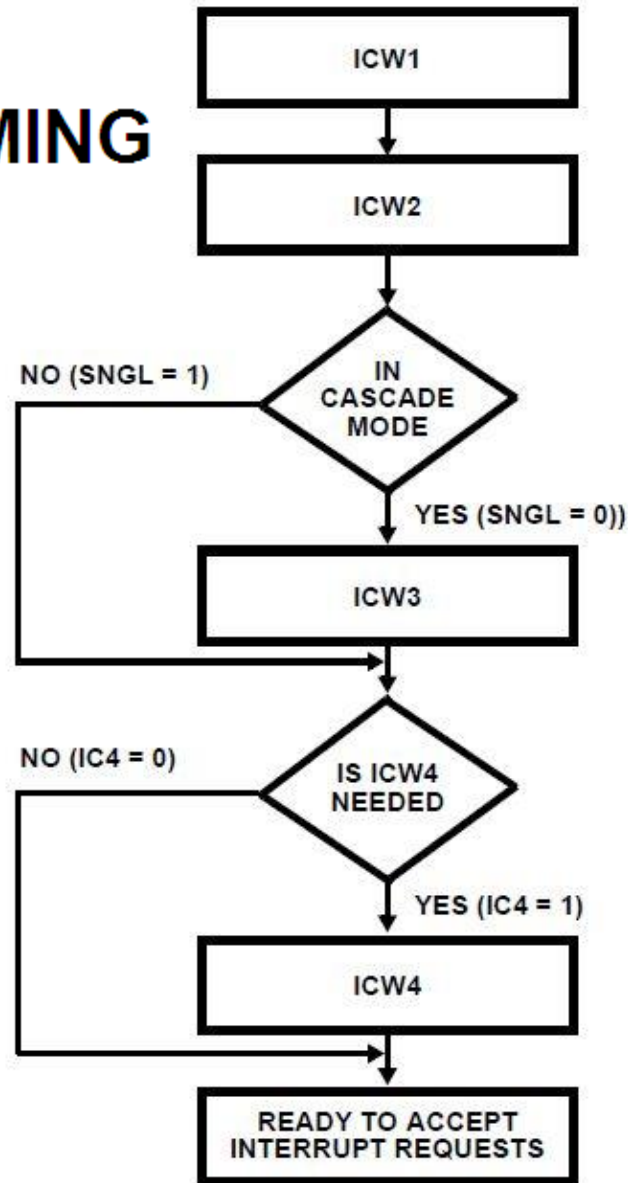
Interrupt Identif. Register

0	0	0	0	ID	ID	ID	PN
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82C59A (PIC)

- **BLOKOVÁ SCHÉMA**
- **JEDNOÚROVNOVÝ SYSTÉM**
- **DVOJÚROVŇOVÝ SYSTÉM**
- **TROJÚROVŇOVÝ SYSTÉM**

8259A PROGRAMMING



ICW1

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	A ₇	A ₆	A ₅	1	LTIM	ADI	SNGL	IC4

- 1 = ICW4 needed
0 = No ICW4 needed
- 1 = Single
0 = Cascade Mode
- CALL address interval
1 = Interval of 4
0 = Interval of 8
- 1 = Level triggered mode
0 = Edge triggered mode
- A₇ - A₅ of Interrupt vector address
(MCS-80/85 mode only)

ICW2

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	A ₁₅ T ₇	A ₁₄ T ₆	A ₁₃ T ₅	A ₁₂ T ₄	A ₁₁ T ₃	A ₁₀	A ₉	A ₈

- A₁₅ - A₈ of interrupt vector address
(MCS80/85 mode)
- T₇ - T₃ of interrupt vector address
(8086/8088 mode)

ICW3 (MASTER)

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	S ₇	S ₆	S ₅	S ₄	S ₃	S ₂	S ₁	S ₀

1 = IR input has a slave
0 = IR input does not have a slave

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	0	0	ID ₂	ID ₁	ID ₀

ICW3 (SLAVE)

SLAVE ID (NOTE)

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	SFNM	BUF	M/S	AEOI	μPM

ICW4

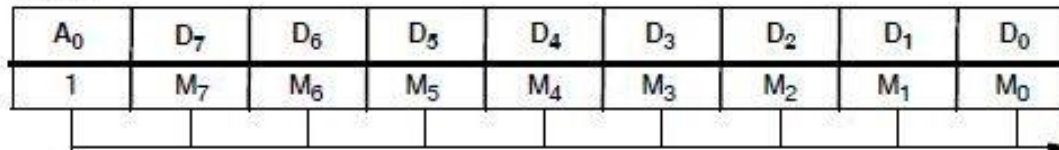
1 = 8086/8088 mode
0 = MCS-80/85 mode

1 = Auto EOI
0 = Normal EOI

0	X	- Non buffered mode
1	0	- Buffered mode slave
1	1	- Buffered mode master

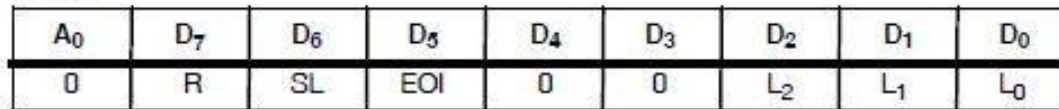
1 = Special fully nested mode
0 = Not special fully nested mode

OCW1



Interrupt Mask
 1 = Mask set
 0 = Mask reset

OCW2



IR LEVEL TO BE
 ACTED UPON

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

0	0	1
0	1	1
1	0	1
1	0	0
0	0	0
1	1	1
1	1	0
0	1	0

- Non-specific EOI command
- † Specific EOI command
- Rotate on non-specific EOI command
- Rotate in automatic EOI mode (set)
- Rotate in automatic EOI mode (clear)
- † Rotate on specific EOI command
- † Set priority command
- No operation

} End of interrupt

} Automatic rotation

} Specific rotation

† L₀ - L₂ are used

OCW3

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	ESMM	SMM	0	1	P	RR	RIS

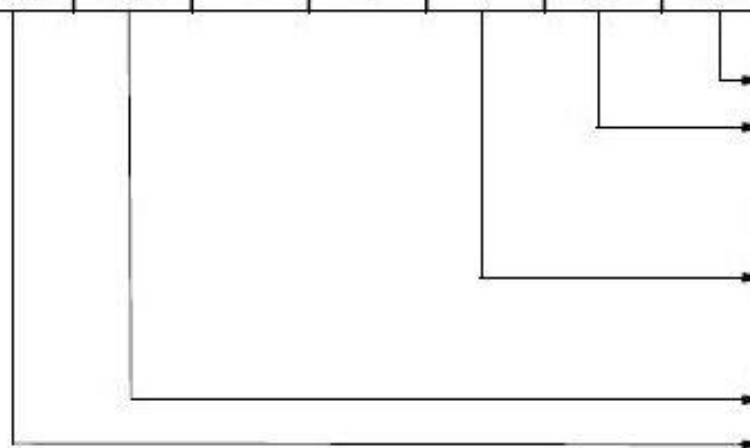
READ REGISTER COMMAND

0	1	0	1
0	0	1	1
No Action		Read IR reg on next RD pulse	Read IS reg on next RD pulse

1 = Poll command
0 = No poll command

SPECIAL MASK MODE

0	1	0	1
0	0	1	1
No Action		Reset special mask	Set special mask



SYSTÉM NA BÁZE 80386EX

- **8254/1: F300H - F303H**
- **8254/2: F304H - F307H**
- **8255/1: F310H - F313H**
- **8255/2: F314H - F317H**
- **16550/1: F380H - F387H**
- **16550/2: F390H - F397H**
- **externý úplný dekóder, overit' M vs. IO priestor**